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SystemVerilog for Verification: A Guide to Learning the Testbench Language Features

Chris Spear

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The updated second edition of this book provides practical information for hardware and software engineers using the SystemVerilog language to verify electronic designs. The author explains methodology concepts for constructing testbenches that are modular and reusable. The book includes extensive coverage of the SystemVerilog 3.1a constructs such as classes, program blocks, randomization, assertions, and functional coverage. This second edition contains a new chapter that covers programs and interfaces as well as chapters with updated information on directed testbench and OOP, layered, and random testbench for an ATM switch.

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